A K-BAND HEMT LOW NOISE RECEIVE MMIC FOR PHASED ARRAY APPLICATIONS

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ABSTRACT

A state-of-the-art InGaAs HEMT receive MMIC consisting of a low noise amplifier and a novel 3-bit phase shifter has been fabricated and evaluated for receive phased-array development at 20 GHz. The low noise amplifier employs series and shunt feedback to provide high gain and low noise performance while the 3-bit phase shifter utilizes a novel switched-allpass approach to minimize circuit size. The monolithic receive chip has demonstrated noise figures of less than 2.75 dB and gains between 11.8 and 14.1 dB for the 8 phase-shift states across the 20.2-21.2 GHz frequency range.

INTRODUCTION

Conformal phased arrays are desirable for airborne and satellite communication systems at extremely high frequencies. Rome Air Development Center [1] has been supporting technology development for 20-GHz receive and 44-GHz transmit monolithic phased arrays. Donn and Bollesen [2] demonstrated an active 16-element receive subarray with 10.9-dBic circular polarization gain at 19.5 GHz. The MESFET receive modules, consisting of a low noise amplifier, a buffer amplifier, and a 3-bit phase shifter achieved an average gain of 5.9 dB at 20 GHz. The objective of this effort is to further reduce the noise figure of the low noise amplifier (LNA) to less than 2.5 dB and to increase gain. The improved noise figure and gain will substantially reduce the number of array elements, the array's complexity, and the cost of phased array antenna systems in the future.

LNA DESIGN

A photograph of the LNA is shown in Figure 1. The physical dimensions of the LNA are 2.0 mm in width and 2.9 mm in length. The first stage utilizes series feedback to obtain both minimum noise figure and optimum input return loss, while the second stage uses shunt and series feedback to achieve gain flatness and good output match. Using feedback also lowers the performance sensitivity to process variations.

A distributed lowpass topology was used to match the 90 μm gate-width HEMT which represents the best compromise between low noise figure and high gain. In addition, a 2 pole low-pass biasing topology consisting of a cascaded LC and RC network was utilized to achieve unconditional stability and minimize the need for external bias circuitry.

PHASE SHIFTER DESIGN

The phase shifter design incorporates a novel switched-allpass approach to minimize the use of long transmission lines while achieving the desired phase shift. The phase of the transmitted signal is shifted by switching between two propagation paths. One path consists of a 50 ohm transmission line and the other path consists of an allpass network embedded between two sections of 50 ohm transmission lines.

A photograph of the 3-bit phase shifter is shown in Figure 2. The physical dimensions of the phase shifter are 2.0 mm in width and 3.8 mm in length. The phase shifter uses 4 HEMTs per phase-shifting bit. A spiral inductor is shunted across the drain-to-source terminals of the HEMT to resonate out its susceptance in the pinch-off state. In addition, a 2000 Ω resistor is used at the gate terminal to isolate the RF signal.

RECEIVE MMIC

The low noise amplifier cascaded with the three-bit phase shifter make up the monolithic receive MMIC. The circuit employs fourteen 0.2 μm T-gate planar doped pseudomorphic InGaAs HEMTs to achieve the low noise figure and high signal gain [3].

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A photograph of the receive MMIC is shown in Figure 3. The physical dimensions of the MMIC are 2.0 mm in width and 6.7 mm in length. A modular integration has been implemented which permits the separation of the individual circuits (LNA or phase shifter) in cases where just one circuit fails to operate. The failed circuit can be replaced with a functioning circuit located elsewhere on the wafer with minimal effect on the module size and bias configurations.

2 X 2 SUBARRAY

The receive MMIC is intended for the 20 GHz phased array development. Figure 4 shows the functional diagram of the 2 X 2 receive subarray while Figure 5 shows the top view of the subarray design including 4 dielectric-filled cavity antennas, 4 HEMT receive MMICs, and a 4-way power combiner. The subarray is arranged in a 2x2 square lattice with a period of 270 mils, which avoids grating lobes up to 21.9 GHz. The cavity receives the incident circularly polarized radiation. The received power excites the cavity slots, couples into the microstrips, and is combined in the Lange coupler which also provides isolation between the antenna and receive module. The signals are then amplified, shifted in phase and enter a 3-dimensional RF feed network that includes 4 miniature coaxes and a 4-way planar power combiner. The coaxes are embedded in the subarray carrier and the combiner is attached on the back side of the carrier.

MEASUREMENT PERFORMANCE

Comprehensive on-wafer measurements were performed on the receive MMIC. The test set-up included the Cascade Microtech on-wafer probe station, ATN noise figure set-up, HP 8510 network analyzer, and HP noise figure meter.

The RF performance of the receive MMIC is shown in Figures 6-9. The module exhibits gains of greater than 11.8 dB, peak-to-peak ripple less than 2.3 dB, and noise figures less than 2.75 dB for all phase states across the 20.2-21.2 GHz frequency band of interest (Figure 6). The phase shift response from 0-360 degrees in increments of 45 degrees shown in Figure 7 has an associated RMS phase error of less than 10 degrees. The input and output VSWR (Figure 8 and 9) is less than 2:1. Figure 10 summarizes the measured performance of the receive MMIC. The total DC power consumption is 40 mW. The DC and RF yield across the wafer was in the neighborhood of 20% and 10% respectively.

CONCLUSION

Compact receive MMICs with greater than 11.8 dB gain, and less than 2.75 dB noise figure for all 8 states of operation have been fabricated using planar doped InGaAs HEMTs. The successful demonstration of the monolithic receive MMIC at 20 GHz encourages phased array development in the future by providing low cost, producible LNA and phase shifter components.

ACKNOWLEDGEMENT

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[2] C. Donn and A.E. Bollesen, "A 16-element K-band Monolithic Active Receive Phased Array Antenna," IEEE AP-S International Symposium Digest, Vol. 1, pp. 188-191, 1988.

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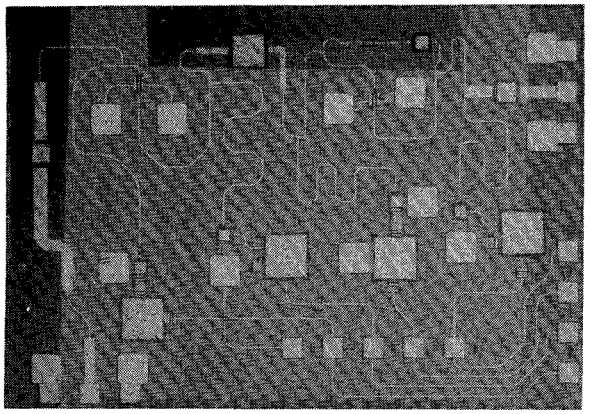

Figure 1. Low Noise Amplifier

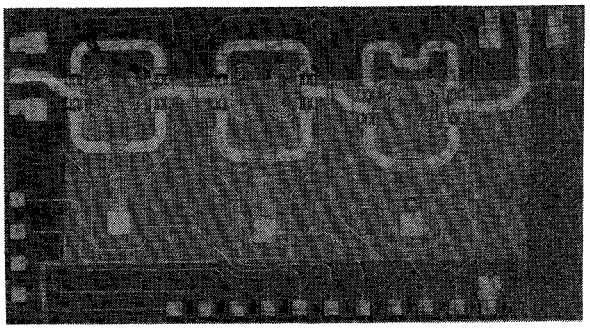

Figure 2. 3-Bit Phase Shifter

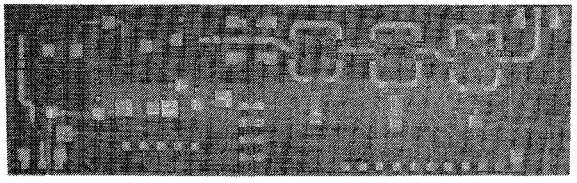

Figure 3. Receive MMIC

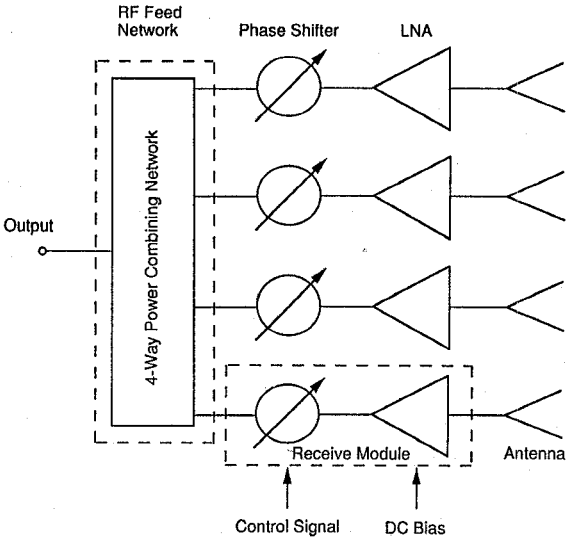

Figure 4. 2X2 Receive Subarray Block

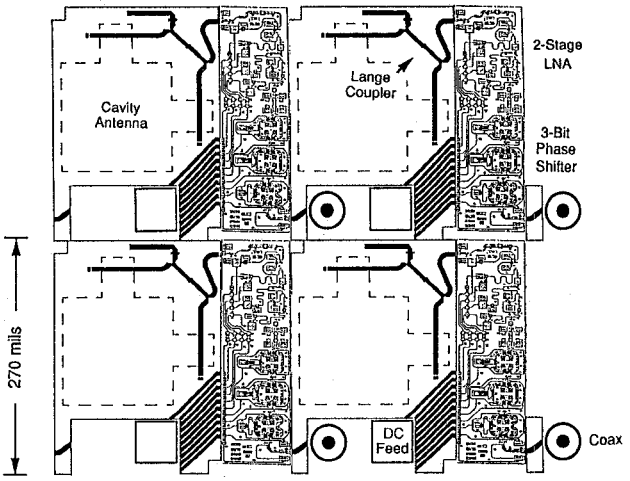

Figure 5. 2X2 Receive Subarray

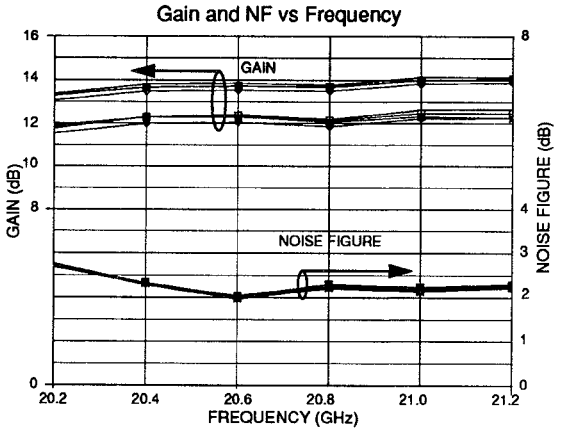

Figure 6. Receive MMIC : Gain and Noise Figure

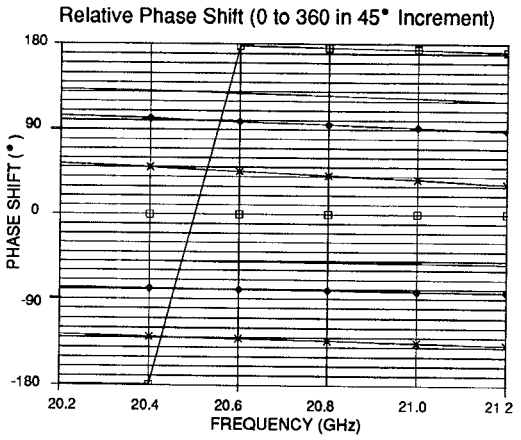

Figure 7. Receive MMIC: Relative Phase Shift

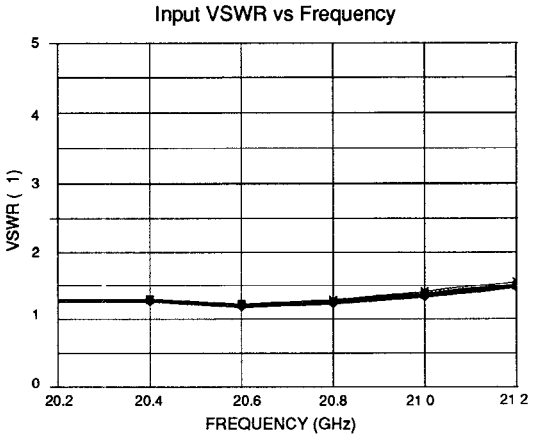

Figure 8. Receive MMIC: Input VSWR

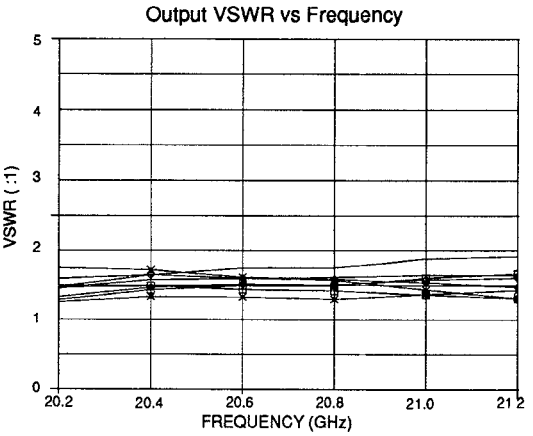

Figure 9. Receive MMIC: Output VSWR

Receive Module Characteristics (8 States)	Frequency (GHz)		
	20.2	20.6	21.2
Average noise figure (dB)	2.7	2.0	2.3
RMS noise figure (dB)	0.1	0.1	0.1
Average gain (dB)	12.5	13.0	13.2
RMS gain (dB)	0.8	0.7	0.8
Average phase error (deg)	4.6	0.9	-5.2
RMS phase error (deg)	8.0	5.8	8.5
Minimum input return loss (dB)	18.0	20.1	13.2
Minimum output return loss (dB)	11.2	11.3	10.0

Figure 10. Receive MMIC Summary